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THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al.  
Serial No.: 10/057,738  
Filed : January 25, 2002  
Assignee : Intel Corporation  
Title : DATA TRANSFER MECHANISM

Art Unit: 2189  
Examiner: Shawn X. Gu

**MAIL STOP AMENDMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information  
Disclosure Statement and documents listed on form PTO-1449.

This filing is being made before the receipt of a first  
Office action on the merits. No fee is required.

The documents are in the English language; hence no concise  
explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the  
return of a copy of the enclosed form PTO-1449 with the

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being  
deposited with the United States Postal Service as first class mail with  
sufficient postage on the date indicated below and is addressed to the  
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

November 27, 2006

Date of Deposit

Signature

Jennifer H. Payne

Typed or Printed Name of Person Signing Certificate

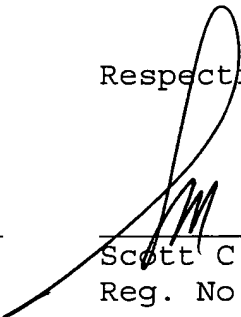
Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Applicants further request consideration of the Information Disclosure Statement submissions filed on June 3, 2004 via the U.S. Patent and Trademark Office's EFS-Web system.

Please apply any additional charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: November 27, 2006



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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-618001	Application No. 10/057,738
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date January 25, 2002	Group Art Unit 2189

### U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

### Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

### Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AQ	Intel, "1A-64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21.
	AR	Paver et al., "Register Locking in Asynchronous Processor Computer Design: VLSI Processors," ICCD '92 Proceedings, IEEE 1992 International Conference, 1992, pp. 351-355.
	AS	
	AT	

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	